WE CLAIM

1. A data processing apparatus, comprising:

a data processing unit for executing instructions;

the data processing unit being responsive to a saturation instruction to apply a saturation operation to a data word Rm comprising a plurality of data values, wherein said saturation operation yields a value given by:

determining from data provided within a field of the saturation instruction a bit position to which saturation is to take place; and

performing in parallel an independent saturation operation on each of the data values to saturate each of the data values to the determined bit position to form a result data word Rd comprising a plurality of saturated data values.

2. A data processing apparatus as claimed in Claim 1, wherein the specified bit position is the same for each of the plurality of data values.

3. A data processing apparatus as claimed in Claim 1, further comprising a source register for storing the data word Rm, and a destination register for storing the result data word Rd.

4. A data processing apparatus as claimed in Claim 1, wherein the data processing unit is arranged on completion of the saturation operation to set a flag if any of the data values were outside of the range of an 'n' bit number corresponding to the determined bit position.

5. A data processing apparatus as claimed in Claim 1, wherein the saturation instruction comprises a signed saturation instruction and the plurality of saturated data values to be produced are signed data values.

6. A data processing apparatus as claimed in Claim 1, wherein the saturation instruction comprises an unsigned saturation instruction and the plurality of saturated data values to be produced are unsigned data values.

7. A data processing apparatus as claimed in Claim 1, wherein the saturation instruction is used in combination with a pack instruction to enable operations to be applied in parallel to selected data values.

8. A data processing apparatus as claimed in Claim 7, wherein the data processing unit is arranged prior to execution of the saturation instruction to be responsive to the pack instruction to perform an operation on a first data word and a second data word, both the first and second data words comprising a number of data values, wherein the operation yields a value given by:

selecting a first data value of said first data word extending from one end of said first data word;

selecting a second data value of said second data word starting from a bit position specified as a shift operand within the pack instruction; and

combining the first and second data values to form respective different data values of said data word Rm.

9. A data processing apparatus as claimed in Claim 1, wherein the saturation instruction is used in combination with an arithmetic instruction to enable operations to be applied in parallel to selected data values.

10. A data processing apparatus as claimed in Claim 9, wherein the data processing unit is arranged prior to execution of the saturation instruction to be responsive to the arithmetic instruction to perform an operation on a first data word and a second data word, wherein the operation yields a value given by:

selecting a plurality of non-adjacent multibit portions of said first data word to form a plurality of multibit portions each of bit length A;

optionally shifting said plurality of multibit portions by a common shift amount to shifted bit positions;

promoting each of said plurality of multibit portions from said bit length of A to a bit length of B to form a plurality of promoted multibit portions, such that said promoted multibit portions may be abutted to form a promoted data word P; and

performing a plurality of independent arithmetic operations using as input operands respective bit position portions of bit length B from both said promoted data word P and said second data word to form said data word Rm comprising a plurality of data values of bit length B.

11. A data processing apparatus as claimed in Claim 1, wherein the data word Rm comprises in a first mode of operation said plurality of data values and in a second mode of operation a single data value, and said data processing unit comprises:

a plurality of logic circuits corresponding to the plurality of data values within the data word Rm in the first mode of operation, each logic circuit being arranged to perform the independent saturation operation on the corresponding data value; and

coupling logic arranged, in said second mode of operation, to cause the plurality of logic circuits to operate together to saturate the single data value.

12. A data processing apparatus as claimed in Claim 11, wherein each logic circuit comprises a selector for selecting the corresponding data value if that corresponding data value is within the range of an 'n' bit number corresponding to the determined bit position, or a mask value if that corresponding data value is outside of the range of the 'n' bit number, the mask value being dependent on the determined bit position.

13. A data processing apparatus as claimed in Claim 12, wherein the coupling logic is arranged to be activated in the second mode of operation such that, if a particular logic circuit determines that the mask value should be selected, the coupling logic is arranged to cause each logic circuit processing less significant bits of the data value to select the mask value.

14. A data processing apparatus as claimed in Claim 11, wherein the mode of operation is indicated by a signal received by the coupling logic and derived from the instruction being executed by the data processing unit.

15. A method of operating a data processing apparatus comprising a data processing unit for executing instructions, the method comprising the steps of:

in response to a saturation instruction, causing the data processing unit to apply a saturation operation to a data word Rm comprising a plurality of data values, wherein said saturation operation yields a value given by:

determining from data provided within a field of the saturation instruction a bit position to which saturation is to take place; and

performing in parallel an independent saturation operation on each of the data values to saturate each of the data values to the determined bit position to form a result data word Rd comprising a plurality of saturated data values.

16. A computer program operable to configure a data processing apparatus to perform a method as claimed in Claim 15.

17. A carrier medium comprising a computer program as claimed in Claim 16.